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| --- | --- | --- | --- |
| **Nama** | Edgrant Henderson Suryajaya | **Kode Asisten** | JJ |
| **NPM** | 2206025016 | **Jenis Tugas** | CS |

**Jawaban**

**Part 1**

1. .

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_1 is

    port (

        masuk : in std\_logic\_vector (2 downto 0);

        a, b, c, d, e, f, g : out std\_logic

    );

end entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_1;

architecture rtl of *CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_1* is

    signal varA, varB, varC: std\_logic;

begin

    varA <= masuk(0);

    varB <= masuk(1);

    varC <= masuk(2);

    g <= '1';

    f <= (not varA) or (varB and not varC);

    e <= varA or varB or not varC;

    d <= varA or varC;

    c <= (varA xnor varB) or (varA and not varC);

    b <= (varB and varC) or (not varA and varC) or (varA and not varB and not varC);

    a <= (not varA and varC) or (not varA and varB) or (varB and varC);

end architecture rtl;

1. Gambar simulasi di vhdl

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1. .

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_3 is

    port (

        masuk : in std\_logic\_vector (2 downto 0);

        keluar : out  std\_logic\_vector (6 downto 0)

    );

end entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_3;

architecture rtl of *CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_3* is

begin

    process(masuk)

    begin

        case masuk is

            when "000" => keluar <= "1110100";

            when "001" => keluar <= "1101111";

            when "010" => keluar <= "1110001";

            when "011" => keluar <= "1111011";

            when "100" => keluar <= "1011110";

            when "101" => keluar <= "1011000";

            when "110" => keluar <= "1111100";

            when "111" => keluar <= "1011111";

            when others => keluar <= "0000000";

        end case;

    end process;

end architecture rtl;

1. .

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_3 is

    port (

        masuk : in std\_logic\_vector (2 downto 0);

        keluar : out  std\_logic\_vector (6 downto 0)

    );

end entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_3;

architecture rtl of *CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_1\_3* is

begin

    process(masuk)

    begin

        REPORT "Nomor 4, Edgrant Henderson Suryajaya";

        case masuk is

            when "000" => keluar <= "1110100";

            when "001" => keluar <= "1101111";

            when "010" => keluar <= "1110001";

            when "011" => keluar <= "1111011";

            when "100" => keluar <= "1011110";

            when "101" => keluar <= "1011000";

            when "110" => keluar <= "1111100";

            when "111" => keluar <= "1011111";

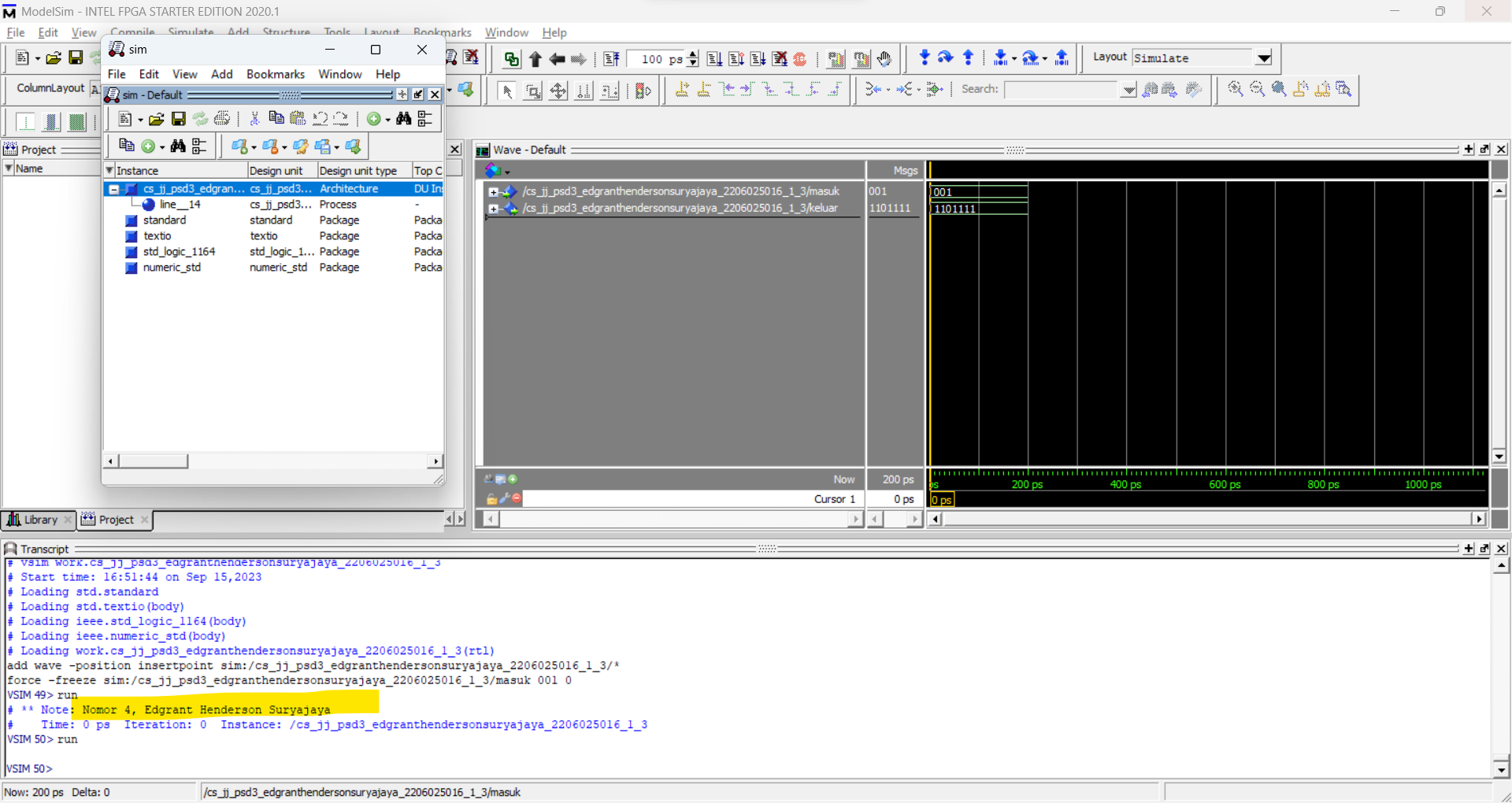
            when others => keluar <= "0000000";

        end case;

    end process;

end architecture rtl;

1. .

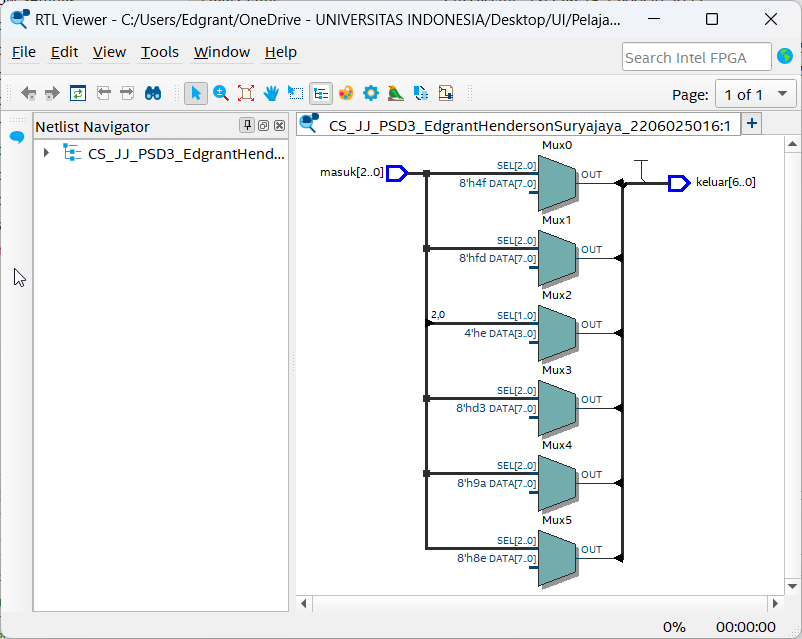


1. Nomor 3, hasil dataflow style

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Nomor 6, hasil behavioural style



1. Rangkaian dataflow syle menggunakan gerbang logika karena memang sudah dibuat setiap persamaannya outputnya menggunakan gerbang logika, sedangkan rangkaian behavioural style menggunakan multiplexer yang dirancang dari switch case pada kode vhdl.
2. Oke bang

**Part 2**

1. npm = 2306475819

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_2\_9 is

    port (

        clk : in std\_logic;

        keluar : out std\_logic\_vector (3 downto 0)

    );

end entity CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_2\_9;

architecture rtl of *CS\_JJ\_PSD3\_EdgrantHendersonSuryajaya\_2206025016\_2\_9* is

begin

    npm\_counter: process(clk)

        variable current\_num : std\_logic\_vector (3 downto 0) := "1001";

    begin

        if falling\_edge(clk) then

            keluar <= current\_num;

            if (current\_num = "1001") then

                current\_num := "0001";

            elsif (current\_num = "0001") then

                current\_num := "1000";

            elsif (current\_num = "1000") then

                current\_num := "0101";

            elsif (current\_num = "0101") then

                current\_num := "0111";

            elsif (current\_num = "0111") then

                current\_num := "0100";

            elsif (current\_num = "0100") then

                current\_num := "0110";

            elsif (current\_num = "0110") then

                current\_num := "0000";

            elsif (current\_num = "0000") then

                current\_num := "0011";

            elsif (current\_num = "0011") then

                current\_num := "0010";

            elsif (current\_num = "0010") then

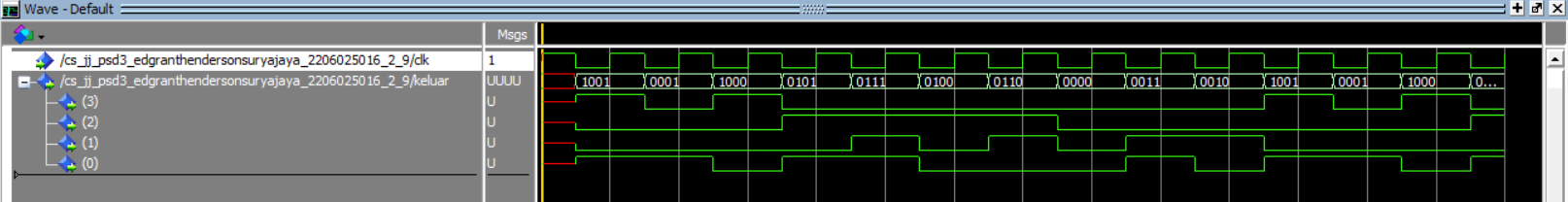
                current\_num := "1001";

            end if;

        end if;

    end process npm\_counter;

end architecture rtl;



1. .

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1. Kesimpulan:
2. Dataflow style dan behavioural style adalah cara penulisan dalam vhdl
   1. Dataflow style menulis hasil dengan gerbang logika
   2. Behavioral style menulis secara sekuensial dan menggunakan conditional statement
3. Implementasi dari dataflow style menggunakan quartus adalah dengan gerbang logika sedangkan behavioral style menggunakan multiplexer
4. Proses digunakan pada behavioral style untuk menunjukan sebuah blok sekuensial
5. Pada proses dapat ada conditional statement. Conditional statement juga dapat merujuk ke state sebelumnya untuk membentuk rangkaian sekuensial